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10/686,420	10/15/2003	Prashant Shamarao	5646-104	7290

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/686,420	SHAMARAO, PRASHANT
	Examiner	Art Unit
	James Sugent	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *27,29 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 27, 29 and 35 are objected to because of the following informalities:

- As to claim 27, reference to "upstream stage" lacks antecedent basis. Examiner asserts applicant intended to refer to "sense amplifier" stated in claim 16. Please change "upstream stage" to "sense amplifier."
- As to claim 29, reference to "downstream stage" lacks antecedent basis. Examiner asserts applicant intended to refer to "clocked output buffer" stated in claim 16. Please change "downstream stage" to "clocked output buffer."
- As to claim 35, reads "...the second driver circuit and the second driver circuit..." (pg. 15, lines 5-6 of claim 35). Examiner asserts applicant intended claim to read "...the second driver circuit and the second receiver circuit..." Please change.

Appropriate correction is required. The above-mentioned requested changes will be applied to the remaining examination for this Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 13-16 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA) in view of Kwak (U.S. Patent No. 6,288,953 B1) (hereinafter referred to as Kwak).

As to claim 1, AAPA discloses a data path, comprising: a downstream stage that strobes data (flip-flop 40) at an input thereof responsive to a first control signal (OCLK), an upstream stage (data receiver 30) that sends data to the input of the downstream stage (as shown in figure 1) responsive to a second control signal (REN) (pg. 1, line 1 thru pg. 2, line 12).

AAPA does not disclose a control circuit operative to fix timing of the second control signal to timing of the first control signal.

Kwak teaches a memory device comprising a control circuit (combination of ATD 140 and sense amplifier control 150) that generates control signals (SACSi and SAL) to sense amplifier (160) and output buffer (170) in response to external address signals (Ai) (column 1, lines 27-56). The control circuit further comprises delay circuits (271-274; column 3, lines 52-65) which repairs timing issues mentioned within the back of the invention (column 1, line 63 thru column 2, line 23).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA and Kwak before him at the time the invention was made, to modify data path disclosed by AAPA to use the control circuit as taught by Kwak.

One of ordinary skill in the art would be motivated to make use of the control circuitry in view of the teachings of Kwak, as doing so would give the added benefit of having a reliable sensing operation in the presence of input noise (column 2, lines 25-30).

As to claim 13, AAPA discloses a data path according wherein the upstream stage (30) comprises a level-enabled data receiver circuit (AAPA discloses that the receiver circuit/upstream circuit [30] is enabled by signal REN. When REN is HIGH, data [RDQOUT] is sent to flip-flop [40]; otherwise, data is held. Therefore, upstream stage is level-enabled; pg. 1, line 9 thru pg. 2, line 12).

As to claim 14, AAPA discloses a data path wherein the level-enabled data receiver circuit (30) comprises a sense amplifier circuit (as shown in figure 1, pg. 1, line 9 thru pg. 2, line 12).

As to claim 15, AAPA discloses a data path wherein the downstream stage (flip-flop 40) comprises a flip-flop circuit (as shown in figure 1, pg. 1, line 9 thru pg. 2, line 12).

As to claim 16, AAPA discloses an integrated circuit memory device, comprising: a clocked output buffer (flip-flop 40) that latches data responsive to a clock signal (OCLK); a sense amplifier (data receiver 30) that passes data (RDQOUT) at an input thereof to an input of the clocked output buffer responsive to an enable signal (REN) (pg. 1, line 9 thru pg. 2, line 12).

AAPA does not disclose a control circuit operative to fix timing of the second control signal to timing of the first control signal.

Kwak teaches a memory device comprising a control circuit (combination of ATD 140 and sense amplifier control 150) that generates control signals (SACSi and SAL) to sense amplifier (160) and output buffer (170) in response to external address signals (Ai) (column 1, lines 27-56). The control circuit further comprises delay circuits (271-274; column 3, lines 52-65) that repairs timing issues mentioned within the back of the invention (column 1, line 63 thru column 2, line 23).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA and Kwak before him at the time the invention was made, to modify data path disclosed by AAPA to use the control circuit as taught by Kwak.

One of ordinary skill in the art would be motivated to make use of the control circuitry in view of the teachings of Kwak, as doing so would give the added benefit of having a reliable sensing operation in the presence of input noise (column 2, lines 25-30).

As to claim 27, AAPA discloses a device wherein the sense amplifier (40) comprises a level-enabled data receiver circuit(AAPA discloses that the receiver circuit/upstream circuit [30] is enabled by signal REN. When REN is HIGH, data [RDQOUT] is sent to flip-flop [40]; otherwise, data is held. Therefore, upstream stage is level-enabled; pg. 1, line 9 thru pg. 2, line 12).

As to claim 28, AAPA discloses a device wherein the level-enabled data receiver circuit (30) comprises a sense amplifier circuit (pg. 1, line 9 thru pg. 2, line 12).

As to claim 29, AAPA discloses a device wherein the clocked output buffer (flip-flop 40) comprises a flip-flop circuit (as shown in figure 1; pg. 1, line 9 thru pg. 2, line 12).

As to claim 30, AAPA discloses a method of operating a data path, the method comprising: strobing data at an input of a downstream stage (flip-flop 40) of the data path responsive to a first control signal (OCLK); sending data (RDQOUT) to the input of the downstream stage (via data receiver 30) responsive to a second control signal (REN) (pg. 1, line 9 thru pg. 2, line 12).

AAPA does not disclose fixing timing of the second control signal to timing of the first control signal.

Kwak teaches a memory device comprising a control circuit (combination of ATD 140 and sense amplifier control 150) that generates control signals (SACSi and SAL) to sense amplifier (160) and output buffer (170) in response to external address signals (Ai) (column 1, lines 27-56). The control circuit further comprises delay circuits (271-274; column 3, lines 52-65) that repairs timing issues mentioned within the back of the invention (column 1, line 63 thru column 2, line 23).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA and Kwak before him at the time the invention was made, to modify data path disclosed by AAPA to use the control circuit as taught by Kwak.

One of ordinary skill in the art would be motivated to make use of the control circuitry in view of the teachings of Kwak, as doing so would give the added benefit of having a reliable sensing operation in the presence of input noise (column 2, lines 25-30).

Claims 35 and 37-39 rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. Patent No. 5, 068,831) (hereinafter referred to as Hoshi) in view of Ohta et al. (U.S. Patent No. 6,192,003 B1) (hereinafter referred to as Ohta).

As to claim 35, Hoshi discloses a method of characterizing a data path comprising a first driver-receiver pair (sense amplifiers 23 and 24) including a first driver circuit (23) and a first receiver circuit (24) and a second driver-receiver pair (sense amplifiers 21 and 22) comprising a second driver circuit (21) and a second receiver circuit (22) wherein the data rate can be increased or decreased and timing issues can be altered via control circuits (equalization circuits 41 and 42) thereby minimizing delay time between sense amplifiers (column 3, lines 48-68 and column 6, lines 15-44).

Hoshi does not disclose the method comprising: controlling an enable signal for the first driver circuit to timing of an enable signal for the first receiver circuit and controlling an enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit; and controlling an enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit and controlling an enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit.

Ohta teaches a memory device timing circuit wherein a timing control circuit (21) is responsible for delaying various control signals (RALCT, RDENT, SAET, CALCT, OELCT and OUTLCT) in a cascading manner via delay circuits (as shown in figure 2) dependent on the previous signal (column 4, lines 43-62; column 5, line 19 thru column 6, line 46).

It would have been obvious to one of ordinary skill of the art, having the teachings of Hoshi and Ohta before him at the time the invention was made, to modify the equalization circuits disclosed by Hoshi to use the timing control circuit as taught by Ohta.

One of ordinary skill in the art would be motivated to make use of timing control circuit in view of the teachings of Ohta, as doing so would give the added benefit of having latency of only 1 clock cycle (column 2, lines 30-36).

As to claim 37, Ohta teaches a method wherein fixing timing of an enable signal (RALCT) for the first driver circuit (14) to timing of an enable signal (RDENT) for the first receiver circuit (13) comprises providing a fixed delay (102) between the enable signal for the first driver circuit and the enable signal for the first receiver circuit; wherein fixing timing of an enable signal (CALCT) for the second receiver circuit (15) to timing of a data strobe signal (OUTLCT) for a stage downstream of the second receiver circuit (17) comprises providing a

fixed delay (113) between the enable signal for the second receiver circuit and the data strobe signal for the downstream stage; wherein fixing timing of the enable signal (RDENT) for the first receiver (13) circuit to timing of an enable signal (SAET) for the second driver circuit (12) comprises providing a fixed delay (106) between the enable signal for the first receiver circuit and the enable signal for the second driver circuit; and wherein fixing timing of the enable signal (SAET) for the second driver circuit (12) to timing of the enable signal (CALCT) for the second receiver circuit (15) comprises providing a fixed delay (107 or 110) between the enable signal for the second driver circuit and the enable signal for the second receiver circuit (column 5, line 15 thru column 6, line 46).

As to claim 38, Hoshi discloses method wherein the first and second driver circuits (21 and 23) and the first and second receiver circuits (22 and 24) comprise respective sense amplifiers (column 6, lines 15-44).

As to claim 39, Hoshi does not disclose a method wherein the downstream stage (25) comprises a flip-flop. AAPA teaches a memory device data path wherein the downstream stage (40) is a flip-flop (pg. 1, line 9 thru pg. 2, line 12).

Claims 2-8, 17-22 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA) and Kwak (U.S. Patent No. 6,288,953 B1) (hereinafter referred to as Kwak) as applied to claims 1, 16 and 30 above, and further in view of Hamamoto et al. (U.S. Patent No. 6,757,212 B2) (hereinafter referred to as Hamamoto).

As to claim 2, AAPA discloses a data path wherein the upstream stage (30) comprises a first upstream stage (20), and wherein the data path further comprises a second upstream stage

(10) that sends data to an input of the first upstream stage (DQOUT) responsive to a third control signal (DEN) (pg. 1, line 9 thru pg. 2, line 12). However, AAPA does not disclose having timing with respect to the second control signal that varies responsive to a frequency at which data is transferred along the data path.

Hamamoto teaches memory device comprising control signals (FCLK and LCLK) that drive circuits (200 and 210) within a data path wherein control signal LCLK is adjusted according to the frequency of the internal clock signal (column 42, lines 14-30).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA, Kwak and Hamamoto before him at the time the invention was made, to modify the control circuitry disclosed by Kwak to use the control signal variance as taught by Hamamoto.

One of ordinary skill in the art would be motivated to make use of the control signal timing scheme in view of the teachings of Hamamoto, as doing so would optimize the internal data reading timing stably at high speeds (column 7, lines 8-21).

As to claim 3, AAPA discloses data path wherein a time interval between assertion of the third control signal and assertion of the second control signal decreases responsive to an increase in the frequency at which the data is transferred along the data path (As in known in the art, frequency and time have a direct proportionate relationship [f=1/t] in that if frequency were to increase, time [response time] would decrease and vice versa; pg. 1, line 9 thru pg. 2, line 12).

As to claim 4, Kwak teaches data path wherein the control circuit (140 and 150) comprises a fixed delay (271-274) circuit that generates the first control signal from the second control signal (column 3, lines 52-65).

As to claim 5, Hamamoto teaches data path wherein the fixed delay circuit comprises a fixed delay circuit in a forward path of a delay locked loop (DLL) or a phase locked loop (PLL) (Hamamoto teaches the clock signal [LCLK] is phase-adjusted therefore, comprising a PLL; column 42, lines 14-30).

As to claim 6, Kwak teaches a data path wherein the control circuit is further operative to selectively fix timing of the second control signal to one of timing of the first control signal and timing of the third control signal (column 7, line 27 thru column 2, line 23).

As to claim 7, Kwak teaches a data path wherein the control circuit comprises a first fixed delay circuit operative to generate the first control signal from the second control signal and a second fixed delay circuit operative to generate the second control signal from the third control signal (Kwak teaches the noise filter [220] has the same configuration as that disclosed in noise filter [12] thus both providing a delay from node to node secondary to the circuit characteristics as is known in the art; column 1, lines 43-56 and column 3, lines 8-51).

As to claim 8, Kwak teaches data path wherein the control circuit is operative to allow relative timing of the third control signal with respect to the second control signal to vary with the frequency at which the data is transferred along the data path when timing of the second control signal is fixed to timing of the first control signal (Kwak teaches the summator [10] receiving pulses correspondingly dependent on the variation of the address signals therefore, producing varying frequencies; column 1, lines 43-56).

As to claim 17, APAA discloses a device wherein the sense amplifier (30) comprises a first sense amplifier, wherein the enable signal (REN) comprises a first enable signal, and further comprising a second sense amplifier (10) that sends the data to an input of the first sense

amplifier (via delay circuit 20) responsive to a second enable (DEN) but does not disclose the signal having a timing with respect to the first enable signal that varies responsive to a rate at which the data is transferred through the first and second sense amplifiers (pg. 1, line 9 thru pg. 2, line 12).

Hamamoto teaches memory device comprising control signals (FCLK and LCLK) that drive circuits (200 and 210) within a data path wherein control signal LCLK is adjusted according to the frequency of the internal clock signal (column 42, lines 14-30).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA, Kwak and Hamamoto before him at the time the invention was made, to modify the control circuitry disclosed by Kwak to use the control signal variance as taught by Hamamoto.

One of ordinary skill in the art would be motivated to make use of the control signal timing scheme in view of the teachings of Hamamoto, as doing so would optimize the internal data reading timing stably at high speeds (column 7, lines 8-21).

As to claim 18, Kwak teaches device wherein the control circuit comprises a fixed delay (271-274) circuit that generates the clock signal from the first enable signal (column 3, lines 52-65).

As to claim 19, Hamamoto teaches a device wherein the fixed delay circuit comprises a fixed delay circuit in a forward path of a DLL circuit or a PLL circuit (Hamamoto teaches the clock signal [LCLK] is phase-adjusted therefore, comprising a PLL; column 42, lines 14-30).

As to claim 20, Kwak teaches a device wherein the control circuit is further operative to selectively fix timing of the first enable signal to one of timing of the clock signal and timing of the second enable signal (column 7, line 27 thru column 2, line 23).

As to claim 21, Kwak teaches a device according to Claim 20, wherein the control circuit comprises a first fixed delay circuit operative to generate the clock signal from the first enable signal and a second fixed delay circuit operative to generate the first enable signal from the second enable signal (Kwak teaches the noise filter [220] has the same configuration as that disclosed in noise filter [12] thus both providing a delay from node to node secondary to the circuit characteristics as is known in the art; column 1, lines 43-56 and column 3, lines 8-51).

As to claim 22, Kwak teaches a device wherein the control circuit is operative to allow relative timing of the second enable signal with respect to the first enable signal to vary with the frequency at which the data is transferred through the first and second sense amplifiers when timing of the first enable signal is fixed to timing of the clock signal (Kwak teaches the summator [10] receiving pulses correspondingly dependent on the variation of the address signals therefore, producing varying frequencies; column 1, lines 43-56).

As to claim 31, AAPA discloses a method wherein the upstream stage (30) comprises a first upstream stage (20), and further comprising sending data (DQOUT) from a second upstream stage (10) to an input of the first upstream stage responsive to a third control signal (DEN) but does not disclose such that timing of the third control signal with respect to the second control signal varies responsive to a frequency at which data is transferred along the data path (pg. 1, line 9 thru pg. 2, line 12).

Hamamoto teaches memory device comprising control signals (FCLK and LCLK) that drive circuits (200 and 210) within a data path wherein control signal LCLK is adjusted according to the frequency of the internal clock signal (column 42, lines 14-30).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA, Kwak and Hamamoto before him at the time the invention was made, to modify the control circuitry disclosed by Kwak to use the control signal variance as taught by Hamamoto.

One of ordinary skill in the art would be motivated to make use of the control signal timing scheme in view of the teachings of Hamamoto, as doing so would optimize the internal data reading timing stably at high speeds (column 7, lines 8-21).

As to claim 32, AAPA discloses a method wherein the first and second upstream stages (10 and 30) comprise respective first and second sense amplifiers (pg. 1, line 9 thru pg. 2, line 12).

As to claim 33, AAPA discloses a method wherein the downstream stage (40) comprises a flip-flop (pg. 1, line 9 thru pg. 2, line 12).

As to claim 34, Hamamoto teaches a method wherein fixing timing of the second control signal (REN) to timing of the first control signal (OCLK) comprises fixing timing of the second control signal to timing of the first control signal while transferring data (RDQOUT) through the data path at rate greater than a predetermined threshold rate, and further comprising fixing timing of the second control signal to timing of the third control signal while transferring data through the data path a rate less than the predetermined threshold rate (Hamamoto teaches the problem wherein the clock signals are generated based upon a predetermined delay time and altering the signals based upon the data rate and clock frequencies; column 4, lines 56-65 and column 32, lines 19-30).

Claims 9-12 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA), Kwak (U.S. Patent No.

6,288,953 B1) (hereinafter referred to as Kwak) and Hamamoto et al. (U.S. Patent No. 6,757,212 B2) (hereinafter referred to as Hamamoto) as applied to claims 2 and 17 above, and further in view of Ohta et al. (U.S. Patent No. 6,192,003 B1) (hereinafter referred to as Ohta).

As to claim 9, AAPA does not disclose a data path wherein the data path comprises a third upstream stage that sends data to the second upstream stage responsive to a fourth control signal; and wherein the control circuit is further operative to fix timing of the fourth control circuit to timing of the third control signal.

Ohta teaches a memory device comprising a downstream output latch (17), an upstream circuit (15) further comprising a first upstream circuit (15), a second upstream circuit (12) and a third upstream circuit (13) wherein the third upstream circuit is responsive to a fourth control signal (RDENT) that sends data to the second upstream circuit (12) wherein the control circuit (21) is further operative to fix timing of the fourth control circuit to timing of the third control signal (column 4, lines 43-62; column 5, line 19 thru column 6, line 46).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA, Kwak, Hamamoto and Ohta before him at the time the invention was made, to modify the number of upstream circuits disclosed by AAPA to use the additional upstream circuit as taught by Ohta.

One of ordinary skill in the art would be motivated to make use of the additional upstream circuit in view of the teachings of Ohta, as doing so would give the added benefit of having low latency of only 1 clock cycle even in high-speed circuits (column 2, lines 30-36).

As to claim 10, Ohta teaches a data path wherein the control circuit (21) comprises a fixed delay circuit (106) operative to generate the third control signal (SAET) from the fourth control signal (RDENT) (column 5, line 19 thru column 6, line 46).

As to claim 11, Ohta teaches data path wherein the data path comprises a fourth upstream stage (14) that sends data to an input of the third upstream stage (13) responsive to a fifth control signal (RALCT); and wherein the control circuit (21) is further operative to selectively fix timing of the fourth control signal (RDENT) to one of timing of the fourth control signal or timing of the fifth control signal (via control signal PMLCT from circuit 22; column 5, line 19 thru column 6, line 46).

As to claim 12, Ohta teaches a data path wherein the control circuit (21) is further operative to fix timing of the second control signal (CALCT) to one of timing of the first control signal (OUTLCT) or timing of the third control signal (SAET) (column 5, line 19 thru column 6, line 46).

As to claim 23, AAPA discloses a second sense amplifier (10) but does not disclose the device further comprising a third sense amplifier that sends data to the second sense amplifier responsive to a third enable signal, and wherein the control circuit is further operative to fix timing of the third enable signal to timing of the second enable signal.

Ohta teaches a memory device comprising a downstream output latch (17), an upstream circuit (15) further comprising a first upstream circuit (15), a second upstream circuit (12) and a third upstream circuit (13) wherein the third upstream circuit is responsive to a fourth control signal (RDENT) that sends data to the second upstream circuit (12) wherein the control circuit

(21) is further operative to fix timing of the fourth control circuit to timing of the third control signal (column 4, lines 43-62; column 5, line 19 thru column 6, line 46).

It would have been obvious to one of ordinary skill of the art, having the teachings of AAPA, Kwak, Hamamoto and Ohta before him at the time the invention was made, to modify the number of upstream circuits disclosed by AAPA to use the additional upstream circuit as taught by Ohta.

One of ordinary skill in the art would be motivated to make use of the additional upstream circuit in view of the teachings of Ohta, as doing so would give the added benefit of having low latency of only 1 clock cycle even in high-speed circuits (column 2, lines 30-36).

As to claim 24, Ohta teaches a device wherein the control circuit (21) comprises a fixed delay circuit (106) operative to generate the second enable signal (SAET) from the third enable signal (RDENT) (column 5, line 19 thru column 6, line 46).

As to claim 25, Ohta teaches a device further comprising a fourth sense amplifier (14) that sends data to an input of the third sense amplifier (13) responsive to a fourth enable signal (RALCT); and wherein the control circuit (21) is further operative to selectively fix timing of the third enable signal (RDENT) to one of timing of the second enable signal or timing of the fourth enable signal (via control signal PMLCT from circuit 22; column 5, line 19 thru column 6, line 46).

As to claim 26, Ohta teaches a device wherein the control circuit (21) is further operative to fix timing of the second control signal (CALCT) to one of timing of the first control signal (OUTLCT) or timing of the third control signal (SAET) (column 5, line 19 thru column 6, line 46).

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. Patent No. 5, 068,831) (hereinafter referred to as Hoshi) and Ohta et al. (U.S. Patent No. 6,192,003 B1) (hereinafter referred to as Ohta) as applied to claim 35 above, and further in view of Harrison et al. (U.S. Patent No. 6,011,732) (hereinafter referred to as Harrison).

As to claim 36, Hoshi does not disclose increasing a rate at which data is passed through the data path to determine a minimum delay between the first driver circuit and the first receiver circuit or increasing a rate at which data is passed through the data path to determine the minimum delay between the first driver circuit and the first receiver circuit.

Harrison teaches a synchronous clock generator to be used in conjunction with a memory device wherein the clock generating device frequency can be increased and deceased thereby varying delays within the delay circuits (40) and achieving minimum and maximum delay times (column 5, lines 30-54).

It would have been obvious to one of ordinary skill of the art, having the teachings of Hoshi, Ohta and Harrison before him at the time the invention was made, to modify the control circuitry disclosed by Ohta to add the delay circuits and phase detectors as taught by Harrison.

One of ordinary skill in the art would be motivated to make use of the delay circuits and phase detectors in view of the teachings of Harrison, as doing so would give the added benefit of monitoring temperature of the circuit (column 3, lines 15-25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
Patent Examiner, Art Unit 2116
February 3, 2006

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